What is claimed is:

1. A trench corner effect, bidirectional flash memory cell comprising:
a trench formed in a silicon substrate;
at least a corner of a first and second side of the trench having a trapping material;
an oxide material filling the trench;
a plurality of active areas located on the silicon substrate substantially adjacent to the first and second sides; and
a control gate above the trench.

2. The memory cell of claim 1 wherein the trapping material has an oxide-nitride-oxide architecture.

3. The memory cell of claim 1 wherein the trapping material is deposited on the first and second sides of the trench.

4. The memory cell of claim 1 wherein the trapping material traps electrons.

5. The memory cell of claim 1 wherein the control gate overlaps at least a portion of each active area.

6. The memory cell of claim 1 wherein a first active area of the plurality of active areas is a drain area and a second active area is a source area.

7. A trench corner effect, bidirectional flash memory cell comprising:
a trench formed in a silicon substrate;
an oxide material filling the trench;
a first and second side of the trench comprising a trapping material between the oxide material and the silicon substrate;

a drain region located on the silicon substrate substantially adjacent to the first side of the trench near the trapping material;

a source region located on the silicon substrate substantially adjacent to the second side of the trench near the trapping material; and

a control gate over the trench such that the control gate and oxide material overlap at least a portion of the drain and source regions.

8. The memory cell of claim 7 wherein the substrate is comprised of a p-type conductive material and the drain and source regions are comprised of an n-type conductive material.

9. The memory cell of claim 7 wherein the substrate is comprised of an n-type conductive material and the drain and source regions are comprised of a p-type conductive material.

10. The memory cell of claim 7 wherein the trapping material on the first side stores a first data bit and the trapping material on the second side stores a second data bit.

11. A trench corner effect, bidirectional flash memory cell comprising:

a trench formed in a silicon substrate;

at least a corner of a first and second side of the trench having a trapping material;

an oxide material in the trench;

a plurality of active areas located on the silicon substrate, each active area substantially adjacent to the first and second sides; and

a control gate above the trench such that the control gate and oxide material overlap at least a portion of the active areas and also such that a portion of the control gate extends into the trench.

12. A trench corner effect, bidirectional flash memory cell comprising:

a trench formed in a silicon substrate;

at least a corner of a first and second side of the trench having a trapping material;
an oxide material in the trench;
a plurality of active areas located on the silicon substrate, each active area substantially adjacent to the first and second sides; and
a control gate within the trench substantially adjacent to the trapping material.

13. The memory cell of claim 12 wherein the oxide material is between the control gate and the trapping material.

14. A trench corner effect, bidirectional flash memory cell comprising:
a trench formed in a silicon substrate;
at least a corner of a first and second side of the trench having a trapping material;
an oxide material filling the trench;
a plurality of active areas located on the silicon substrate, each active area substantially adjacent to an opening of the trench and substantially adjacent to the first and second sides;
a first control gate part above the trench such that the control gate and oxide material overlap at least a portion of the active areas; and
a second control gate part within the trench substantially adjacent to the trapping material.

15. The memory cell of claim 14 wherein the oxide material is between the second control gate part and the trapping material.

16. A method for programming a trench corner effect, bidirectional flash memory cell comprising a trench in a substrate, first and second active areas, a control gate, and an oxide-nitride-oxide structure along a first and second side of the trench, the method comprising:
applying a voltage to the substrate that is less than or equal to 0V;
applying a voltage to the control gate that is less than or equal to 0V;

applying a voltage to the first active area that is substantially equal to 0V; and

programming a first bit by applying a positive voltage to the second active area such that charges are moved from the second active area to the nitride material in a corner of the second side of the trench.

17. The method of claim 16 wherein the positive voltage applied to the second active area is substantially in a range of 6.0 – 8.5V.

18. The method of claim 16 and further including programming a second bit by applying a voltage that is substantially equal to 0V to the second active area and the positive voltage to the first active area such that charges are moved from the first active area to the nitride material in a corner of the first side of the trench.

19. The method of claim 16 and further including applying a positive substrate voltage to accelerate charge trapping in the silicon-oxide interface.

20. The method of claim 16 and further including applying a negative voltage to the control gate.

21. A method for reading a plurality of bits from a trench corner effect, bidirectional flash memory cell comprising a trench in a substrate, first and second active areas, a control gate, and a nitride-oxide interface along a first and second side of the trench, the method comprising:

applying a first positive voltage to the control gate that is greater than 0V and is sufficient to create a first energy barrier at the nitride-oxide interface of the first side and a second energy barrier at the nitride-oxide interface of the second side;

applying a second positive voltage to the first active area such that the first energy barrier is either reduced or eliminated in response to a first charge at the first side nitride-oxide interface; and

reading a first bit of the plurality of bits if the first energy barrier is eliminated.

22. The method of claim 21 and further including:

applying the second positive voltage to the second active area such that the second energy barrier is either reduced or eliminated in response to a second charge at the second side nitride-oxide interface; and

reading a second bit of the plurality of bits if the second if the second energy barrier is eliminated.

23. The method of claim 21 wherein the first energy barrier is reduced by the second positive voltage if the first charge is not present and eliminated if the first charge is present.

24. The method of claim 21 wherein the second energy barrier is reduced by the second positive voltage if the second charge is not present and eliminated if the second charge is present.